Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1-55 (canceled)

Claim 56 (currently amended): A method of manufacturing a semiconductor light emitting element having a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, the method comprising:

growing a first semiconductor layer of the first conduction type on a substrate;

forming a growth mask having an opening at a predetermined position on the first semiconductor layer;

selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask;~~ and~~

sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer~~.~~; and

removing the growth mask between selectively growing the second semiconductor layer of the first conduction type on the first semiconductor layer

exposed through the opening in the growth mask and sequentially growing at least the active layer and the semiconductor layer of the second conduction type.

Claim 57 (previously presented): The method of manufacturing a semiconductor light emitting element according to claim 56 wherein the growth mask includes a lamination of at least one of silicon nitride, silicon oxide nitride and silicon oxide.

Claim 58 (previously presented): The method of manufacturing a semiconductor light emitting element according to claim 56 wherein at least the surface of the growth mask includes silicon nitride.

Claim 59 (previously presented): The method of manufacturing a semiconductor light emitting element according to claim 56 wherein the size of the opening in the growth mask ranges from about 2 μm to about 13 μm.

Claim 60 (previously presented): The method of manufacturing a semiconductor light emitting element according to claim 56 wherein the crystal portion has a wurtzite crystal structure.

Claim 61 (previously presented): The method of manufacturing a semiconductor light emitting element according to claim 56 wherein the crystal portion includes a nitride III-V compound semiconductor.

Claim 62 (previously presented): The method of manufacturing a semiconductor light emitting element according to claim 56 wherein the semiconductor layer of the first conduction type, the first semiconductor layer, the second semiconductor layer, the active layer and the semiconductor layer of the second conduction type include nitride III-V compound semiconductors.

Claim 63 (previously presented): The method of manufacturing a semiconductor light emitting element according to claim 59 wherein the crystal planes composing the inclined crystal plane are S-oriented planes.

Claim 64 (previously presented): The method of manufacturing a semiconductor light emitting element according to claim 60 wherein the angles of inclination of the crystal planes composing the inclined crystal plane is stepwise smaller from a bottom of the crystal portion toward an apex thereof.

Claim 65 (previously presented): The method of manufacturing a semiconductor light emitting element according to claim 56 wherein the crystal portion is steeple-shaped.

Claim 66 (previously presented): The method of manufacturing a semiconductor light emitting element according to claim 56 wherein the crystal portion has a six-sided steeple configuration.

Claim 67 (previously presented): The method of manufacturing a semiconductor light emitting element according to claim 56 wherein the crystal portion is elongate in a direction parallel to the major surface.

Claim 68 (previously presented): The method of manufacturing a semiconductor light emitting element according to claim 56 wherein growth temperature for the selective growth is controlled and from about 920°C to about 960°C.

Claim 69 (previously presented): The method of manufacturing a semiconductor light emitting element according to claim 56 wherein a growth rate for the selective growth is controlled at about 6 μm/h or greater.

Claim 70 (previously presented): The method of manufacturing a semiconductor light emitting element according to claim 56 wherein the growth temperature for the active layer and the semiconductor layer of the second conduction type is set lower than the growth temperature for selective growth of the second semiconductor layer.

Claim 71 (previously presented): The method of manufacturing a semiconductor light emitting element according to claim 56 wherein after the second semiconductor layer is selectively grown to have a crystal plane substantially parallel to the major surface on the top thereof, an undoped semiconductor layer is grown on the top of the second semiconductor layer.

Claims 72-73 (canceled)

Claim 74 (currently amended): A method of manufacturing an integrated semiconductor light emitting device integrating a plurality of integrated light emitting elements each having a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on

the crystal portion and electrically connected to the semiconductor layer of the second conduction type, the method comprising:

growing a first semiconductor layer of the first conduction type on a substrate;

forming a growth mask having openings at predetermined positions on the first semiconductor layer;

selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the openings in the growth mask; ~~and~~

sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer~~.~~; and

removing the growth mask between selectively growing the second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask and sequentially growing at least the active layer and the semiconductor layer of the second conduction type.

Claim 75 (previously presented): The method of manufacturing an integrated semiconductor light emitting device according to claim 74 wherein a size of each opening in the growth mask ranges from about 4/1 to about 1 time a size of each semiconductor light emitting element.

Claim 76 (previously presented): The method of manufacturing an integrated semiconductor light emitting device according to claim 74 wherein a distance between nearest two of the openings is equal to or more than two times the size of each semiconductor light emitting element.

Claim 77 (previously presented): The method of manufacturing an integrated semiconductor light emitting device according to claim 74 wherein a size of each opening in the growth mask ranges from about 2 μm to about 13 μm.

Claim 78 (previously presented): The method of manufacturing an integrated semiconductor light emitting device according to claim 74 wherein a distance between nearest two of the openings is equal to or more than about 10 μm.

Claim 79 (canceled)

Claim 80 (currently amended): A method of manufacturing an image display device integrating a plurality of integrated light emitting elements each having a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

growing a first semiconductor layer of the first conduction type on a substrate;

forming a growth mask having openings at predetermined positions on the first semiconductor layer;

selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the openings in the growth mask; ~~and~~

sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer~~.~~; and

removing the growth mask between selectively growing the second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask and sequentially growing at least the active layer and the semiconductor layer of the second conduction type.

Claim 81 (canceled)

Claim 82 (currently amended): A method of manufacturing an illuminating device having a single semiconductor light emitting element or a plurality of integrated semiconductor light emitting elements each including a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

growing a first semiconductor layer of the first conduction type on a substrate;

forming a growth mask having an opening at a predetermined position on the first semiconductor layer;

selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask; ~~and~~

sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer~~.~~; and

removing the growth mask between selectively growing the second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask and sequentially growing at least the active layer and the semiconductor layer of the second conduction type.

Claim 83 (canceled)

Claim 84 (currently amended): A method of manufacturing a semiconductor light emitting element having a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, the method comprising:

growing a first semiconductor layer of the first conduction type on a substrate;

forming a growth mask having an opening at a predetermined position on the first semiconductor layer;

selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask; ~~and~~

sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.; and

removing the growth mask between selectively growing the second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask and sequentially growing at least the active layer and the semiconductor layer of the second conduction type.

Claim 85 (canceled)

Claim 86 (currently amended): A method of manufacturing an integrated semiconductor light emitting device including a plurality of integrated semiconductor light emitting elements each having: a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an

inclined crystal plane exhibiting a substantially convex plane; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, the method comprising:

growing a first semiconductor layer of the first conduction type on a substrate;

forming a growth mask having openings at predetermined positions on the first semiconductor layer;

selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the openings in the growth mask; ~~and~~

sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.; and

removing the growth mask between selectively growing the second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask and sequentially growing at least the active layer and the semiconductor layer of the second conduction type.

Claim 87 (canceled)

Claim 88 (currently amended): A method of manufacturing an image display device integrating a plurality of integrated light emitting elements each having a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on

the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, the method comprising:

growing a first semiconductor layer of the first conduction type on a substrate;

forming a growth mask having openings at predetermined positions on the first semiconductor layer;

selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the openings in the growth mask; ~~and~~

sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer~~.~~; and

removing the growth mask between selectively growing the second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask and sequentially growing at least the active layer and the semiconductor layer of the second conduction type.

Claim 89 (canceled)

Claim 90 (currently amended): A method of manufacturing an illuminating device having a single semiconductor light emitting element or a plurality of integrated semiconductor light emitting elements each including: a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, the method comprising:

growing a first semiconductor layer of the first conduction type on a substrate;

forming a growth mask having an opening at a predetermined position on the first semiconductor layer;

selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask; ~~and~~

sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer~~.~~; and

removing the growth mask between selectively growing the second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask and sequentially growing at least the active layer and the semiconductor layer of the second conduction type.